Application No. 10/756,777
Supplemental Reply to Office Action of September 12, 2005

Amendments to the Drawings:

The attached formal drawing sheet replaces the original sheet of formal drawings.

Fig. 1: Add a "sensing circuit" shown within dashed lines.

Attachment: Replacement Drawing Sheet (1 sheets)

REMARKS

Claims 1-30 are pending. Claims 1 and 6 were amended. Withdrawal of all claim rejections is respectfully requested for at least the reasons set forth below.

Examiner Telephone Calls

The Examiner telephoned Applicants' undersigned representative on December 27, 2005 to discuss whether certain issues can be resolved to place the application in condition for allowance. Follow-up telephone calls were held on January 9 and 10, 2006 to discuss a proposed version of the present Supplemental Amendment. The items discussed in the telephone calls are addressed below.

Agreement was reached on January 10, 2006 that the proposed Supplemental Amendment would place the application in condition for allowance, and that Applicants would promptly fax file the Supplemental Amendment.

Drawing Amendment

The Examiner pointed out that the comparator in claims 1 and 6 was not shown in the figures as required by PTO rules. Upon review, it was discovered that the comparator was accidentally left out of Fig. 1. The attached replacement sheet for Fig. 1 shows the comparator.

No new matter was added in amending Fig. 1. The originally filed text fully supports the additional sensing circuit that shows the decoder/driver 2 and the comparator 3. See, for example, the following text portions of the original specification (which includes the originally filed claims):

1. Paragraph [034] on page 9: FIG 1 is a block diagram of a system according to one embodiment of the present invention, which is not necessarily drawn to scale, in which the dimensions of various components may be arbitrarily increased or reduced. The system according to this particular embodiment comprises a comparator 3 receiving a reference current or voltage (I.sub.ref or V.sub.ref), driver 2 (which can also be a decoder), and nonvolatile memory (PHINES 10).

2. Paragraph [061] spanning pages 25-26: For reading the bits in the nonvolatile memory, a bias voltage will be applied. A threshold voltage V_t or read current I_{read} will be detected in sensing and reading the nonvolatile memory. Driver 2 and comparator 3 (shown in FIG. 1 in conjunction with PHINES 10) will be used in sensing and reading the nonvolatile memory.

3. Claims 1 and 6: ...a comparator receiving a first input resulting from the read current and a second input in a form of one of a reference voltage and a reference current...

4. Claim 25: ...one of the reference voltage and the reference current is provided in a sensing circuit having a driver and a comparator...

Claim Amendments

a. Claim 1

The Examiner requested that the phrase, "either side of the trapping layer of" be added between the words "in" and "the" in the paragraph that reads "the trapping layer being operable..." to improve the clarity of the claim. Applicants have amended claim 1 accordingly.

The Examiner stated that he now believes that the phrase, "at least one bit" in Fig. 1 is confusing. The Examiner suggested that claim 1 be amended to recite the more specific language in claim 6 that refers to "one of a drain bit and a source bit."

In response, Applicants do not wish to amend claim 1 in this manner because the amended claim 1 would then be identical in scope to claim 6. Instead, Applicants propose to amend claim 1 to clarify that the nonvolatile memory ha[s] at least one bit. In this manner, there is a clear antecedent basis for the subsequent recitation that "the trapping layer [is] operable to retain electrons in an erase state for at least one bit in the nonvolatile memory." The specification fully supports this amendment. The nonvolatile memory is described throughout the specification as having at least one bit. See, for example, the following text portions of the specification (which includes the originally filed claims):

1. Paragraph [057] spanning pages 23-24: Once the bits in the nonvolatile memory are erased or programmed, at least one bit will be read and sensed in obtaining information stored therein. A method for operating a nonvolatile memory having at least one bit according to one embodiment of the present invention comprises erasing the at least one bit by retaining electrons

in a nitride layer, programming the at least one bit by injecting electric holes (or by electron reduction), reading the at least one bit by applying a bias voltage, detecting a threshold voltage or a read current for the at least one bit, providing a reference voltage or a reference current, comparing the threshold voltage with the reference voltage or comparing the read current with the reference current. The at least one bit is erased if the threshold voltage is larger than the reference voltage or the read current is lower than the reference current. The at least one bit is programmed if the threshold voltage is lower than the reference voltage or the read current is larger than the reference current.

2. Claim 16: A method for operating a nonvolatile memory having at least one bit comprising...

b. Claim 6

The Examiner did not highlight any deficiencies in the language of claim 6. However, in reviewing the claims, an antecedent basis problem was discovered in claim 6 and is corrected in the currently amended version of claim 6.

Patentability of claim 1 over U.S. Patent No. 5,659,503 (Sudo et al.)

Upon re-review, the Examiner questioned whether at least claim 1 is patentable over Sudo et al. (hereafter, "Sudo"), taken alone. In the outstanding rejection, claim 1 was rejected over Applicants' prior U.S. patent in combination with Sudo, and a terminal disclaimer was filed to overcome this rejection. The Examiner now questioned whether Sudo discloses the claim limitations that Applicants' prior U.S. patent was previously relied upon for disclosing.

In the outstanding Office Action, the Examiner relied upon Sudo only for the claimed comparator (comparing circuit 8 in Sudo). Assuming, arguendo, that the comparing circuit 8 is equivalent to the claimed comparator, Applicants do not agree that the nonvolatile memory in Sudo discloses the remaining limitations of claim 1. Column 1, lines 18-20 of Sudo merely discloses that the nonvolatile memory is "formed of...an electrically erasable programmable field effect transistor such as a floating gate field effect transistor..." Nowhere does Sudo

disclose or suggest a nonvolatile memory that has the specific structure recited in claim 1, which reads as follows:

> a nonvolatile memory having at least one bit and further comprising a p type semiconductor substrate, a first isolation layer over the p type semiconductor substrate, a trapping layer over the first isolation layer, a second isolation layer over the trapping layer, a gate over the second isolation layer, two N+ junctions in the p type semiconductor substrate, and a source and a drain respectively formed on the N+ junctions

Applicants thus do not believe that a rejection under 35 U.S.C. § 102(b) or § 103(a) can be supported by Sudo.

Conclusion

Insofar as the Examiner's rejections were fully addressed, the instant application is in condition for allowance. A Notice of Allowability of all pending claims is therefore earnestly solicited.

Respectfully submitted,

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(Date)

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Enclosures

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